AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at line 10 on page 19 of the substitute specification with the following rewritten paragraph.

A reproduction-signal processing section 106 fetches a signal component corresponding to the data that is recorded in the optical disk 101 from a reproduction signal, binarizes the fetched signal to binary data, generates ~~fieldd~~ a read clock in accordance with the binary data and a reference clock, by using a built-in PLL (Phase Locked Loop) (not illustrated), and reproduces read data synchronizing with the read clock.

Please replace the paragraph beginning at line 20 on page 19 of the substitute specification with the following rewritten paragraph.

A format encoder/decoder 107 reproduces the address information that is recorded in the optical disk 101 in accordance with the ~~fieldd~~ read clock and read data output from the reproduction signal processing section 106, and generates and supplies various timing signals which are necessary for recording or reproducing at the timing synchronized with a sector of the optical disk 101 based on the position of the reproduced address information. It is possible to record or reproduce data at a correct timing by outputting a timing signal such as ~~fieldd~~ read gate signal which is necessary for binarization of an address or data or PLL processing to the reproduction signal processing section 106 at the time of reproduction, or by outputting a timing signal such as a write gate signal for allowing light emission of a recording power to the laser driving section 108 at the time of recording.

Please replace the paragraph beginning at line 11 on page 20 of the substitute specification with the following rewritten paragraph.

An address-mark detection section 111 detects an address mark (AM) which is recorded in an address field by using the ~~fieldd~~read clock and read data supplied from the reproduction signal processing section 106. A demodulation section 112 demodulates address information and user data by using the ~~fieldd~~read clock and read data supplied from the reproduction signal processing section 106. An address-error

detection section 113 detects errors in the address information (address demodulation data) demodulated by the demodulation section 112. A timing generation section 114 secures the synch with a sector format by using an address-mark detection timing signal by the address-mark detection section 111 and a timing signal detecting that there is no error in address information by the address-error detection section 113, and generates a timing signal necessary for recording or reproducing data. Details of the operations of the sections above described will be described later.

Please replace the paragraph beginning at line 1 on page 21 of the substitute specification with the following rewritten paragraph.

Moreover, when recording data, the format encoder/decoder 107 adds a redundant data parity such as an error correction code to user data supplied from an external unit through a host interface 109, and outputs write data which is modulated by a built-in modulation section 115 in accordance with a predetermined format to the laser driving section 108. Moreover, when reproducing data, the format encoder/decoder 107 performs demodulation and error correction of the data recorded in the optical disk 101 in accordance with the ~~fieldd~~read clock and read data output from the reproduction signal processing section 106, and transmits the corrected data to an external unit through the host interface 109.

Please replace the paragraph beginning at line 10 on page 26 of the substitute specification with the following rewritten paragraph.

First, an address-mark detection section 111 detects a pattern of an address mark recorded in each address mark field (AM) shown in Fig. 2 by using a ~~fieldd~~read clock RCLK and read data RD supplied from the reproduction signal processing section 106, and outputs an AM detection pulse AMDP at the timing of detecting the address mark.

Please replace the paragraph beginning at line 15 on page 26 of the substitute specification with the following rewritten paragraph.

A demodulation section 112 demodulates address-information-error-detecting-and-encoding data corresponding to address information and an error detection code

recorded in an address information field (PID) and an error detection code field (IED), respectively, that is, (address information + error detection code) by using ~~fieldd~~ the read clock RCLK and read data RD, and generates and outputs address demodulation data ADMD. When generating the address demodulation data ADMD corresponding to (address information + error detection code), the demodulation section 112 refers to the AM detection pulse AMDP as the timing for generating the address demodulation data ADMD and starts demodulation by using read data RD corresponding to the following (address information + error detection code) in accordance with the timing of the AM detection pulse AMDP.

Please replace the paragraph beginning at line 8 on page 43 of the substitute specification with the following rewritten paragraph.

The timing generation section 114 in Fig. 8 has a function of generating a timing signal such as ~~fieldd~~read gate signal RGS which is required to reproduce data. The timing generation section 114 is constituted of a reference-clock generation section 301, a sector sync counter 302, a counted-value (counter value) decoder 303, and a counted-value (counter value) correction section 304. Each of these functional blocks is described below.

Please replace the paragraph beginning at line 24 on page 43 of the substitute specification with the following rewritten paragraph.

Moreover, in contrast to the case of recording, it is unnecessary to greatly suppress the jitter component of a clock because the jitter is not related to a quality of recording data. Because a timing signal that is required to reproduce data is generated by using the reference clock REFCLK2, it is permitted to use a frequency corresponding to a linear velocity. Therefore, it is also permitted to use the ~~fieldd~~read clock RCLK output by the reproduction signal processing section 106 as the reference clock REFCLK2.

Please replace the paragraph beginning at line 18 on page 45 of the substitute specification with the following rewritten paragraph.

Figs. 9A to 9C are timing charts for explaining the timing generating operation of the counted-value decoding section 303 in this embodiment. In Fig. 9, the ~~fielddread~~ gate signal RGS serves as a gate signal for allowing the reproduction-signal processing section 106 to binarize a reproduction signal and to perform the PLL operation synchronizing with binarized data. By performing operations such as binarization and PLL only when the read gate signal RGS is kept H-level, it is possible to prevent an unnecessary reproducing operation from being performed at a portion in which data is not recorded and the operations are effective for the stabilization of a read clock and the reduction of power consumption. The counted-value decoder 303 decodes the output CT02 shown in Fig. 9A in a sector for reproducing data and thereby keeps the read gate signal RSG shown in Fig. 9B H-level while the counter output CT02 has a value from c7 to (c10-1). Hereby, it is possible to perform a binarization and PLL operation by the reproduction-signal processing section 106 in a period from the c7 channel bit to the c10 channel bit from the head of a sector for reproducing data.

Please replace the paragraph beginning at line 3 on page 52 of the substitute specification with the following rewritten paragraph.

Moreover, when the counted-value decoder 403 receives a ~~fielddread~~ enable signal RENBL from the recording/reproducing control section 405 when reproducing data, the counted-value decoder 403 outputs a ~~fielddread~~ gate signal RGS to a reproduction-signal processing section 106, and moreover, generates a window signal WNS, which is necessary for the detection of a pre-sync code and the demodulation of data, and outputs the signal WNS to the demodulation section 112. Because the details of timing signal generation when reproducing data are the same as the contents described in Fig. 9, a description of the details thereof is omitted here. The counted-value decoder 403 also generates an AM detection window signal AMDWNS and feeds the signal AMDWNS back to the counted-value correction section 404.

Please replace the paragraph beginning at line 22 on page 52 of the substitute specification with the following rewritten paragraph.

The recording/reproducing control section 405 receives a recording command RECCOM from a system controller 110 when recording data and outputs a write enable signal WENBL in accordance with a predetermined criterion. Moreover, the recording/reproducing control section 405 receives a reproduction command REPCOM from the system controller 110 when reproducing data and outputs a ~~fielddread~~ enable signal RENBL in accordance with a predetermined criterion. Output algorithms of a write enable signal WENBL and ~~fielddread~~ enable signal RENBL in each sector, that is, the conditions for allowing data to be recorded and reproduced in each sector, will be described later.